WHAT IS CLAIMED IS:

1. An interprocessor communication method of exchanging the contents of register files among processors constituting a multiprocessor system, comprising the steps of:

dividing a group of processors constituting the multiprocessor system into a plurality of groups of processing elements,

conducting interprocessor communication by physically sharing the same register file among processors belonging to the same processing element, and

conducting interprocessor communication by directly transferring the contents of a register file through a bus between processors belonging to different processing elements.

2. The interprocessor communication method as set forth in claim 1, wherein

a bus is used which has a channel one-to-one corresponding to each register included in the register file.

3. The interprocessor communication method as set forth in claim 1, wherein

a bus having a channel whose number is smaller than the number of registers included in the register

file is used to enable a plurality of registers to share one channel.

4. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of buses and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge.

5. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of local buses, not less than one global bus and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one local bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge.

6. The interprocessor communication method as set

forth in claim 1, wherein

a bus structure formed of a plurality of buses and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge, and

not less than one route which connects the processing elements by a bus and causes no bus contention with other routes is determined in advance to conduct only interprocessor communication using the determined route.

7. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of local buses, not less than one global bus and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one local bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge, and

not less than one route which connects the processing elements by a bus and causes no bus contention with other routes is determined in advance to conduct only interprocessor communication using the determined route.

8. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of buses and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge, and

not less than one route which connects the processing elements by a bus and causes no time contention on the same bus with other routes and a time of use of each bus by each route are determined in advance to time-divisionally use the buses, thereby conducting only interprocessor communication using said determined route and time of use.

9. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of local buses, not less than one global bus and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one local bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge, and

not less than one route which connects the processing elements by a bus and causes no time contention on the same bus with other routes and a time of use of each bus by each route are determined in advance to time-divisionally use the buses, thereby conducting only interprocessor communication using said determined route and time of use.

10. The interprocessor communication method as set forth in claim 8, wherein

the processors are operated in synchronization with time and each processor is programmed to execute only the interprocessor communication by said determined route and time of use, and each bridge conducts data relay operation only in the interprocessor communication by said determined route and time of use, thereby time-divisionally using the buses.

11. The interprocessor communication method as set forth in claim 8, wherein

a transmission control unit for controlling transmission of the contents of the register file in the processing element through the bus according to a transmission request from the processor belonging to the processing element in question provides control such that only interprocessor communication by said determined route and time of use is conducted and each bridge executes data relay operation only in interprocessor communication by said determined route and time of use, thereby time-divisionally using the buses.

12. The interprocessor communication method as set forth in claim 8, wherein

a time table for conducting input/output control by time is provided in the processing element and a time table for conducting relay control by time is provided in the bridge, and input/output control at the processing element and path control at the bridge are determined uniquely with respect to time by using these time tables, and

when a transmission request is made from the processor, a transmission control unit in the processing element refers to the time table based on time to conduct output control of data from the register to the

bus, the bridge refers to the time table based on time to conduct relay processing of data between the buses and a reception control unit in the processing element refers to the time table based on time to conduct input control of data from the bus to the register, thereby time-divisionally using the buses.

13. The interprocessor communication method as set forth in claim 8, wherein

a connection table for conducting input/output control by a connection number or a data destination and a time table for conducting input/output control by time are provided in the processing element, a connection table for conducting relay control by the connection number or the data destination is provided in the bridge, and a control channel for transmitting the connection number or the data destination as control information is provided in the bus, and

at the time of outputting data from the processor, a transmission request is made with the connection number or the destination as control information, a transmission control unit in the processing element refers to the connection table and the time table based on the control information to conduct output control of data and control information to the buses, the bridge refers to the connection table based on the control information received from the control channel to conduct

relay processing of data and control information between the buses and a reception control unit in the processing element refers to the connection table based on the received control information to conduct input control of data from the bus to the register, thereby

time-divisionally using the buses.

14. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of buses and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge, and

not less than one route which connects the processing elements by a bus and causes no contention on the same channel of the same bus with other routes is determined in advance to space-divisionally use the buses on a channel basis, thereby conducting only interprocessor communication using said determined route.

15. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of local buses, not less than one global bus and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one local bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge, and

not less than one route which connects the processing elements by a bus and causes no contention on the same channel of the same bus with other routes is determined in advance to space-divisionally use the buses on a channel basis, thereby conducting only interprocessor communication using said determined route.

16. The interprocessor communication method as set forth in claim 14, wherein

each processor is programmed to execute only the interprocessor communication by said determined route, and each bridge conducts data relay operation only in the interprocessor communication by said determined route, thereby

space-divisionally using the buses.

17. The interprocessor communication method as set forth in claim 14, wherein

a transmission control unit for controlling transmission of the contents of the register file in the processing element through the bus according to a transmission request from the processor belonging to the processing element in question provides control such that only interprocessor communication by said determined route is conducted and each bridge executes data relay operation only in interprocessor communication by said determined route, thereby

space-divisionally using the buses.

18. The interprocessor communication method as set forth in claim 14, wherein

a connection table for conducting input/output control is provided for each channel in the processing element and a connection table for conducting relay control is provided for each channel in the bridge, and input/output control at the processing element and path control at the bridge are determined for each channel by using these connection tables, and

at the time of outputting data from the processor, not less than one register is selected to make a transmission request, a transmission control unit in the processing element refers to the connection table related to a channel corresponding to each register to which the transmission request is made to conduct output control of data from each register to the bus on a

channel basis, the bridge refers to the connection table related to each channel to conduct relay processing of data between the buses for each channel and a reception control unit in the processing element refers to the connection table related to each channel to conduct input control of data from the bus to the register for each channel, thereby

space-divisionally using the buses.

19. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of buses and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge, and

not less than one route which connects the processing elements by a bus and causes no time contention on the same channel of the same bus with other routes and a time of use of a channel of each bus by each route are determined in advance to time-divisionally and space-divisionally use the buses on a channel basis, thereby conducting only interprocessor

communication using said determined route and time of use.

20. The interprocessor communication method as set forth in claim 1, wherein

a bus structure formed of a plurality of local buses, not less than one global bus and a bridge for relaying data between the buses is used, in which a group of processing elements is divided into a plurality of groups, communication between processing elements belonging to the same group is conducted through the same one local bus and communication between processing elements belonging to different groups is conducted through a plurality of buses using the bridge, and

not less than one route which connects the processing elements by a bus and causes no time contention on the same channel of the same bus with other routes and a time of use of a channel of each bus by each route are determined in advance to time-divisionally and space-divisionally use the buses on a channel basis, thereby conducting only interprocessor communication using said determined route and time of use.

21. The interprocessor communication method as set forth in claim 19, wherein

the processors are operated in synchronization

with time and each processor is programmed to execute only the interprocessor communication by said determined route and time of use, and each bridge conducts data relay operation only in the interprocessor communication by said determined route and time of use, thereby

time-divisionally and space-divisionally using the buses.

22. The interprocessor communication method as set forth in claim 19, wherein

a transmission control unit for controlling transmission of the contents of the register file in the processing element through the bus according to a transmission request from the processor belonging to the processing element in question provides control such that only interprocessor communication by said determined route and time of use is conducted and each bridge executes data relay operation only in interprocessor communication by said determined route and time of use, thereby

time-divisionally and space-divisionally using the buses.

23. The interprocessor communication method as set forth in claim 19, wherein

a time table for conducting input/output control by time is provided for each channel in the processing

element and a time table for conducting relay control by time is provided for each channel in the bridge, and input/output control at the processing element and path control at the bridge are determined for each channel uniquely with respect to time by using these time tables, and

when a transmission request is made from the processor, a transmission control unit in the processing element refers to each time table based on time to conduct output control of data from the register to the bus on a channel basis, the bridge refers to each time table based on time to conduct relay processing of data between the buses on a channel basis and a reception control unit in the processing element refers to each time table based on time to conduct input control of data from the bus to the register on a channel basis, thereby

time-divisionally and space-divisionally using the buses.

24. The interprocessor communication method as set forth in claim 19, wherein

a connection table for conducting input/output control by a connection number or a data destination and a time table for conducting input/output control by time are provided in the processing element, a connection table for conducting relay control by the connection

number or the data destination is provided in the bridge, and a control channel for transmitting the connection number or the data designation as control information is provided for each channel in the bus, and

at the time of outputting data from the processor, a transmission request is made with the connection number or the destination as control information, a transmission control unit in the processing element refers to each connection table and each time table based on control information to conduct output control of data and control information to the buses on a channel basis, the bridge refers to each connection table based on the control information received from the control channel to conduct relay processing of data and control information between the buses on a channel basis and a reception control unit in the processing element refers to each connection table based on the received control information to conduct input control of data from the bus to the register on a channel basis, thereby

time-divisionally and space-divisionally using the buses.

25. The interprocessor communication method as set forth in claim 19, wherein

a connection table for conducting input/output control by a connection number or a data destination and a time table for conducting input/output control by time

are provided in the processing element, a connection table for conducting relay control by the connection number or the data destination is provided in the bridge, and a control channel for transmitting the connection number or the data designation as control information is provided for each channel in the bus, and

at the time of outputting data from the processor, a transmission request is made with the connection number or the destination as control information, a transmission control unit in the processing element refers to the connection table and the time table based on control information to conduct output control of data and control information to the buses on a channel basis, the bridge refers to each connection table based on the control information received from the control channel to conduct relay processing of data and control information between the buses on a channel basis and a reception control unit in the processing element refers to the connection table based on the received control information to conduct input control of data from the bus to the register on a channel basis, thereby

time-divisionally and space-divisionally using the buses.

26. The interprocessor communication method as set forth in claim 12, wherein

the transmission control unit in each processing

element, after a transmission request is made, inhibits write from the processor into a register relevant to the transmission request until data is actually output onto the bus.

27. The interprocessor communication method as set forth in claim 12, wherein

the contents of a register file scheduled to be received are inhibited from being read and at a time when the reception control unit inputs the data received through the bus into the register file in the processing element, are changed to be readable.

28. A multiprocessor system comprising:

a plurality of processing elements including a plurality of processors physically sharing the same register file, and

a bus structure formed of a local bus for connecting register files of several adjacent processing elements with each other, not less than one global bus for connecting the local buses and not less than one bridge for relaying data between the buses.

29. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel one-to-one corresponding to each register included in the register

file.

30. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel whose number is smaller than the number of the registers included in the register file.

31. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel one-to-one corresponding to each register included in the register file,

the register file of each processing element includes a time table for conducting input/output control by time, a transmission control unit for, when a transmission request is made from the processor, referring to the time table based on time to control output of data from the register to the bus and a reception control unit for referring to the time table based on time to control input of data from the bus to the register, and

each bridge includes a time table for conducting relay control by time and a relay circuit for referring to the time table based on time to conduct relay processing of data between the buses, thereby

forming a structure time-divisionally using buses.

32. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel whose number is smaller than the number of the registers included in the register file,

the register file of each processing element includes a time table for conducting input/output control by time, a transmission control unit for, when a transmission request is made from the processor, referring to the time table based on time to control output of data from the register to the bus and a reception control unit for referring to the time table based on time to control input of data from the bus to the register, and

each bridge includes a time table for conducting relay control by time and a relay circuit for referring to the time table based on time to conduct relay processing of data between the buses, thereby

forming a structure time-divisionally using buses.

33. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel one-to-one corresponding to each register included in the register file,

each bus includes a control channel for

transmitting a connection number or a destination of data as control information,

the register file of each processing element includes a connection table for conducting input/output control by the connection number or the data destination and a time table for conducting input/output control by time, a transmission control unit for, when a transmission request is made from the processor using the connection number or the destination as control information, referring to the connection table and the time table based on the control information to control output of data and control information to the buses, and a reception control unit for referring to the connection table based on control information received from the bus to control input of data from the bus to the register, and

each bridge includes a connection table for conducting relay control by the connection number or the data destination, and a relay control unit and a relay circuit for referring to the connection table based on control information received from the control channel to conduct relay processing of data and control information between the buses, thereby

forming a structure time-divisionally using buses.

34. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel whose number is smaller than the number of the registers included in the register file,

each bus includes a control channel for transmitting a connection number or a destination of data as control information,

the register file of each processing element includes a connection table for conducting input/output control by the connection number or the data destination and a time table for conducting input/output control by time, a transmission control unit for, when a transmission request is made from the processor using the connection number or the destination as control information, referring to the connection table and the time table based on the control information to control output of data and control information to the buses, and a reception control unit for referring to the connection table based on control information received from the bus to control input of data from the bus to the register, and

each bridge includes a connection table for conducting relay control by the connection number or the data destination, and a relay control unit and a relay circuit for referring to the connection table based on control information received from the control channel to conduct relay processing of data and control information between the buses, thereby

forming a structure time-divisionally using buses.

35. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel one-to-one corresponding to each register included in the register file, and

the register file of each processing element includes a connection table for each channel for conducting input/output control, a transmission control unit for, when a transmission request designating a register which conducts transmission is made from the processor, referring to the connection table related to a channel corresponding to each register to which the transmission request is made to control output of data from each register to the bus on a channel basis, and a reception control unit for referring to the connection table related to each channel to control input of data from the bus to the register on a channel basis, and

each bridge includes a connection table for each channel for conducting relay control and a relay circuit for referring to the connection table related to each channel to conduct relay processing of data between the buses, thereby

forming a structure space-divisionally using buses.

36. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel whose number is smaller than the number of the registers included in the register file, and

the register file of each processing element includes a connection table for each channel for conducting input/output control, a transmission control unit for, when a transmission request designating a register which conducts transmission is made from the processor, referring to the connection table related to a channel corresponding to each register to which the transmission request is made to control output of data from each register to the bus on a channel basis, and a reception control unit for referring to the connection table related to each channel to control input of data from the bus to the register on a channel basis, and

each bridge includes a connection table for each channel for conducting relay control and a relay circuit for referring to the connection table related to each channel to conduct relay processing of data between the buses, thereby

forming a structure space-divisionally using buses.

37. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel one-to-one corresponding to each register included in the register file,

the register file of each processing element includes a time table for each channel for conducting input/output control by time, a transmission control unit for, when a transmission request is made from the processor, referring to each time table based on time to control output of data from the register to the bus on a channel basis, and a reception control unit for referring to each time table based on time to control input of data from the bus to the register on a channel basis, and

each bridge includes a time table for each channel for conducting relay control by time and a relay circuit for referring to each time table based on time to conduct relay processing of data between the buses on a channel basis, thereby

forming a structure time-divisionally and space-divisionally using buses.

38. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel whose number is smaller than the number of the registers included in the register file,

the register file of each processing element

includes a time table for each channel for conducting input/output control by time, a transmission control unit for, when a transmission request is made from the processor, referring to each time table based on time to control output of data from the register to the bus on a channel basis and a reception control unit for referring to each time table based on time to control input of data from the bus to the register on a channel basis, and

each bridge includes a time table for each channel for conducting relay control by time and a relay circuit for referring to each time table based on time to conduct relay processing of data between the buses on a channel basis, thereby

forming a structure time-divisionally and space-divisionally using buses.

39. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel one-to-one corresponding to each register included in the register file,

each bus includes a control channel for each channel for transmitting a connection number or a destination of data as control information,

the register file of each processing element includes a connection table for each channel for

conducting input/output control by the connection number or the destination of data and a time table for each channel for conducting input/output control by time, a transmission control unit for, when a transmission request with the connection number or the destination as control information is made from the processor, referring to each connection table and each time table based on the control information to control output of the data and the control information to the bus on a channel basis, and a reception control unit for referring to each connection table based on control information received from the bus to control input of data from the bus to the register on a channel basis, and

each bridge includes a connection table for each channel for conducting relay control by the connection number or the data destination, and a relay control unit and a relay circuit for referring to each connection table based on control information received from the control channel to conduct relay processing of data and the control information between the buses on a channel basis, thereby

forming a structure time-divisionally and space-divisionally using buses.

40. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel whose number is smaller than the number of the registers included in the register file,

each bus includes a control channel for each channel for transmitting a connection number or a destination of data as control information,

the register file of each processing element includes a connection table for each channel for conducting input/output control by the connection number or the destination of data and a time table for each channel for conducting input/output control by time, a transmission control unit, for when a transmission request with the connection number or the destination as control information is made from the processor, referring to each connection table and each time table based on the control information to control output of the data and the control information to the bus on a channel basis, and a reception control unit for referring to each connection table based on control information received from the bus to control input of data from the bus to the register on a channel basis, and

each bridge includes a connection table for each channel for conducting relay control by the connection number or the data destination, and a relay control unit and a relay circuit for referring to each connection table based on control information received from the

control channel to conduct relay processing of data and the control information between the buses on a channel basis, thereby

forming a structure time-divisionally and space-divisionally using buses.

41. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel one-to-one corresponding to each register included in the register file,

each bus includes a control channel for each channel for transmitting a connection number or a destination of data as control information,

the register file of each processing element includes a connection table for conducting input/output control by the connection number or the data destination and a time table for conducting input/output control by time, a transmission control unit for, when a transmission request is made from the processor using the connection number or the destination as control information, referring to the connection table and the time table based on the control information to control output of data and control information to the buses on a channel basis, and a reception control unit for referring to the connection table based on control information received from the bus to control input of

data from the bus to the register on a channel basis, and

each bridge includes a connection table for each channel for conducting relay control by the connection number or the data destination, and a relay control unit and a relay circuit for referring to each connection table based on control information received from the control channel to conduct relay processing of the data and the control information between the buses on a channel basis, thereby

forming a structure time-divisionally and space-divisionally using buses.

42. The multiprocessor as set forth in claim 28, wherein

each said bus has a channel whose number is smaller than the number of the registers included in the register file,

each bus includes a control channel for each channel for transmitting a connection number or a destination of data as control information,

the register file of each processing element includes a connection table for conducting input/output control by the connection number or the data destination and a time table for conducting input/output control by time, a transmission control unit for, when a transmission request is made from the processor using

the connection number or the destination as control information, referring to the connection table and the time table based on the control information to control output of data and control information to the buses on a channel basis, and a reception control unit for referring to the connection table based on control information received from the bus to control input of data from the bus to the register on a channel basis, and

each bridge includes a connection table for each channel for conducting relay control by the connection number or the data destination, and a relay control unit and a relay circuit for referring to each connection table based on control information received from the control channel to conduct relay processing of the data and the control information between the buses on a channel basis, thereby

forming a structure time-divisionally and space-divisionally using buses.

43. The multiprocessor as set forth in claim 31, wherein

the transmission control unit in each processing element has a structure of inhibiting, after a transmission request is made, write from a processor into a register relevant to the transmission request until data is actually output onto the bus.

44. The multiprocessor as set forth in claim 32, wherein

the transmission control unit in each processing element has a structure of inhibiting, after a transmission request is made, write from the processor into a register relevant to the transmission request until data is actually output onto the bus.

45. The multiprocessor as set forth in claim 31, including

a structure of inhibiting read of the contents of a register file scheduled to be received and changing the contents to be readable at a time when the reception control unit inputs the data received through the bus into the register file in the processing element.

46. The multiprocessor as set forth in claim 32, including

a structure of inhibiting read of the contents of a register file scheduled to be received and changing the contents to be readable at a time when the reception control unit inputs the data received through the bus into the register file in the processing element.